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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,114	02/11/2004	Hiroshi Kageyama	NITT.0190	2612

7590 06/28/2005

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EXAMINER	
AL NAZER, LEITH A	

ART UNIT	PAPER NUMBER
2821	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/775,114	KAGEYAMA ET AL.	
	Examiner	Art Unit	
	Leith A. Al-Nazer	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-17* is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/11/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. patent application publication no. 2005/0068270 to Awakura et al.

With respect to claims 1 and 3-6, Awakura teaches an image display device comprising an image display portion (14) in which a plurality of pixels are arranged in a matrix (figure 2); a plurality of signal lines (111 and 112 in figure 2; paragraph 0048) wired in the image display portion to carry a voltage signal to the pixels; and a drive circuit (11) to control voltage on each of the signal lines, wherein each of the pixels comprises a light emitting element (24 in figure 2) and a pixel circuit (341 in figure 16) which controls the intensity of light emission of the light emitting element, the image display device being equipped with a pixel circuit voltage detecting means (17 in figures 2 and 9; 25 in figure 16; paragraph 0048; paragraph 0081) to selectively output a voltage internal to the pixel circuit included in each of the pixels to the signal line to which the pixel circuit connects, and the drive circuit being equipped with a voltage addition means ("Analog Adder" in figure 9) to add the voltage on the signal line and a signal voltage corresponding to image data to be displayed and output a sum voltage to the signal line again (figures 9 and 10).

With respect to claim 2, Awakura teaches the pixel circuit voltage detecting means comprising circuitry which can place the pixel circuit included in each of the pixels in three states: a disconnection state from the signal line (21 in figure 2), a connection state to the signal line (21 in figure 2), and a resistive connection state wherein the pixel circuit connects to the signal line with a sufficiently higher value of resistance than in the connection state (30 in figure 23; paragraphs 0097-0101).

With respect to claim 7, Awakura teaches the light emitting element being a light-emitting diode element (24).

With respect to claim 8, Awakura teaches the pixel circuit and the pixel circuit voltage detecting means being configured with thin-film transistors (paragraph 0048).

With respect to claim 9, Awakura teaches the pixel circuit being configured with either n-channel or p-channel thin-film transistors (paragraph 0048).

Allowable Subject Matter

5. Claims 10-17 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest one or more of the limitations found in independent claim 10. With respect to independent claim 10, the prior art of record fails to teach or suggest the image display further including a plurality of resistive wiring lines having a higher value of resistance than the signal lines and wired in parallel with the signal lines, a plurality of first switching means to control connection between each of the signal lines and each of the resistive wiring lines, and a plurality of second switching means to control connection between each of the resistive wiring lines and each of the pixel circuits.

Citation of Pertinent References

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patent documents further show the state of the art with respect to image display devices:

a. U.S. patent no. 6,323,851 to Nakanishi

b. U.S. patent no. 6,480,189 to Ide

c. U.S. patent application publication no. 2003/0184538 to Yamato et al.

d. U.S. patent application publication no. 2004/0080473 to Higuma et al.

e. U.S. patent application publication no. 2005/0007328 to Yamazaki et al.

f. U.S. patent application publication no. 2005/0062691 to Tamura et al.

g. Japanese patent application publication no. 2000-056847

Communication Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leith A. Al-Nazer whose telephone number is 571-272-1938. The examiner can normally be reached on Monday-Friday, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Don Wong
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Technology Center 2800

LA